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10/660,844	09/12/2003	Joseph M. Jeddeloh	501321.01	7877

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Edward W. Bulchis, Esq.
DORSEY & WHITNEY LLP
Suite 3400
1420 Fifth Avenue
Seattle, WA 98101

EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/660,844	JEDDELOH, JOSEPH M.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/03/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered October 16, 2006.

- Claims 1-50 are pending.
- Claims 11, 19, 32, 36, 42 and 44-45 are amended.
- Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to claims 1-50 filed October 16, 2006 have been fully considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends that prior art of record Lin et al. does not teach a memory hub, a plurality of memory devices and a memory hub that changes the relative timing between the signals. Examiner respectfully disagrees.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., memory devices and memory hub) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Examiner would like to respectfully convey to the Applicant that the definition of hub is "A common connection point for devices in a network." Therefore, given the

broadest possible interpretation of the claim language the limitation of a memory hub is over come by the tester (Fig 1 # 22) in Lin et al. Further, Applicant argues that the memory banks are not equivalent to a plurality of memory devices, since they cannot "be separately accessed...." Examiner would like to respectfully suggest that the claim does not recite the requirement for a memory device to be separately accessible. However, even if the Examiner reads that limitation into the claims, the embodiment of Figures 1 and 2 is just an example and "multiple variations and modifications to the disclosed embodiments will occur" within the scope of the invention. Therefore, Figure 2 can be redrawn eliminating the outline of memory device 26, thus rendering the memory banks to be access able separately through the address latches. Lastly, it may also be incorporated, without departing from the scope of the invention that the tester could be used to test multiple devices of different frequencies (column 10, lines 55-65).

As per the contention that Lin does not teach altering the relative timing of the signals the Examiner would like to cite several passages from Lin et al. "It is noted that the memory device 26 may have multiplexed address terminals. In this situation, addresses may be conveyed to the memory device 26 by first conveying a portion of the x address signals (e.g., a row address portion) during one cycle of the CLOCK1 signal, then conveying a remainder of the x address signals (e.g., a column address portion) during a subsequent cycle of the CLOCK1 signal. Thus, all x address signals of an address may not be conveyed to the memory device 26 at the same time (i.e., during the same cycle of the CLOCK1 signal)." (column 6, lines 55-65) Therefore, there is a timing difference between the address signals.

Further, "As a result of, for example, the address signals being asserted for x cycles of the CLOCK signal, the memory device 26 can be operated at a greater speed relative to the tester 22. Since more of the fixed capacity of the DBM 30 (FIG. 1) can be available for data used for example by the pattern generator 32, relatively large capacity memory devices can be tested in a single pass where testing of the devices would otherwise require 2 or more passes.

In accordance with one aspect of the invention, more of the fixed capacity of the DBM 30 (FIG. 1) may be made available for generation of test pattern data and/or forwarding of data signals to the data comparator 34, by reducing, for example, the number of address signals that must be generated by the tester 22. For example, a relatively large memory device 26 expectedly has a large number of address terminals to receive address signals. In a first part of a testing procedure, one of the address signal bits, e.g., a least significant bit (LSB), may be tied to one logical value (e.g., a logic `0`), allowing the pattern generator 32 to provide one less address signal during the first part of the testing procedure wherein even addresses are generated. In a second part of a testing procedure wherein odd address are generated, the least significant bit of the address signal may be tied to the other logical value (e.g., a logic `1`). As a result, less of the DBM 30 storage capacity is needed to store the data used by the pattern generator 32 to generate the address signals, leaving more of the DBM 30 storage capacity available for other operations and/or higher operating speeds." (column 9, lines 35-60). Therefore, by increasing or decreasing the DBM storage capacity the operating speeds of the signals may be altered.

Also, "and the first clock signal is used to produce a second (test) clock signal having a frequency greater than a frequency of the first clock signal **during an operation** 164 (e.g., the CLOCK signal of FIG. 1). During an operation 166, the test clock signal is provided to a memory device (under test) such that operations within the memory device are synchronized to the test clock signal. For example, in FIG. 1, the CLOCK signal is provided to the memory device 26 such that operations within the memory device 26 are synchronized to the CLOCK signal.

During an operation 168, test data is written to even addresses of the memory device using control, data, and address signals synchronized for example to the first clock signal. **One or more of the signals can instead be synchronized** to the test clock signal in modified embodiments." (column 10, lines 1-28). During an operation refers to the fact that the timings may be changed during the procedure, further one or more signals **may** be synchronized or not, whenever signals are synchronized there relative timing is changed. Lastly, column 12, lines 55-67 display the range of frequencies, which could be used during testing.

As per the 112 rejection, Examiner would like to request Applicant that it is understandable what "relative timing" between two signals means, however in the claim language the way the phrase is used "relative timing **between when**" renders the claim indefinite. There needs to be reference to the signals before when. An example of the modification may be and to alter the relative timing between the first and the second signal, when. Therefore, the 112 rejections are maintained.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-18, 23-31, 36-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1, 11, 23, 36, 42, & 44:

These claims mention the term "relative timing." The term relative is indefinite and it does not clearly point out the subject matter of the invention.

As per claims 2-10, 12-18, 24-31, 37-41, & 43:

These claims are rejected by virtue of its dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-6, 10-11, 13-15, 19 & 22 are rejected under 35 U.S.C. 102 (e) as being fully anticipated by Lin et al. (hereinafter Lin) US Pat no. 6880117 B2.

As per claims 1 & 11:

Lin teaches a memory module, comprising: a plurality of memory devices (Figure 2 # 50A-c); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 26); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device (Figure 4A); and a self-test module (Figure 1 # 22) coupled to at least one of the memory devices, the self-test module being operable to couple a series of corresponding first and second signals to the at least one memory device and to alter the relative timing between when some of the corresponding first and second signals in the series are coupled to the at least one memory device over a range (Figure 1 # 24), the self-test module further receiving output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first and second signals (Figure 1 # 34).

As per claim 3 &13:

Lin teaches the memory module as rejected in claim 1 above wherein the memory hub further comprises a plurality of link interfaces (Figure 2 # 40, 42, 44), a plurality of memory device interfaces (Figure 2 # 50A-C), and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces (column 8, lines 5-60).

As per claim 4 & 14:

Lin teaches the memory module as rejected in claim 1 above wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices (column 2, lines 55-60).

As per claim 5:

Lin teaches the memory module as rejected in claim 1 above wherein the self-test module further comprises: a pattern generator producing a pattern of data bits each of which is used to generate a respective one the first signals in the series (Figure 1 # 32); and a comparator coupled to the pattern generator and to the at least one memory device, the comparator receiving output signals from the at least one memory device and determining a pattern of data corresponding thereto, the comparator further and comparing the pattern generated from the output signals to the pattern of data from which the first signals are generated (Figure 1 # 34).

As per claim 6 & 15:

Lin teaches the memory module as rejected in claim 1 above wherein the self-test module further comprises a storage device coupled to the comparator to store the results of the comparisons between the pattern generated from the output signals and the pattern of data from which the first signals are generated (Figure 1 # 30, column 5, lines 5-40).

As per claim 10:

Lin teaches the memory module as rejected in claim 1 above wherein the self-test module is further operable to couple a signal from the memory device corresponding to each of the output signals and to alter the relative timing between the

signal coupled from the memory device and the corresponding output signal (Figure 1 # 24 & 28).

As per claim 19:

Lin teaches a memory module, comprising: a plurality of synchronous memory devices (Figure 2 # 50A-C); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 26); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device (Figure 1 # 22); and a variable frequency clock generator producing and coupling to the at least one memory device a clock signal having a frequency corresponding to a frequency control signal (Figure 1 # 24); and a self-test module coupled to at least one of the memory devices, the self-test module being operable to generate the frequency control signal so that the frequency of the clock signal varies over a range (Figure 1 # 24, column 4, lines 15-65)), the self-test module further being operable couple a series of first input signals to the at least one memory device and to receive output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first signals as the frequency of the clock signal is varied (Figure 1 # 34).

As per claim 22:

Lin teaches the memory module as rejected in claim 19 above wherein the memory hub further comprises a plurality of link interfaces (Figure 2 # 40, 42, 44), a plurality of memory device interfaces (Figure 2 # 50A-C), and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces (column 8, lines 5-60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2, 9, 12, 16-17, 20-21, 23 & 32 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Lin et al. US Pat no. 6880117 B2.

As per claim 2 & 12, 21:

Lin discloses the claimed invention except for the exact location of the maintenance port. It would have been obvious to one having ordinary skill in the art at

the time the invention was made to place the maintenance port such that it was externally accessible, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

As per claim 9, 16-17, 20:

Lin discloses the claimed invention except for explicitly mentioning the exact composition of the first and second signals. It would have been obvious to one of ordinary skill in the art at the time the invention was made to comprise the first signals with data (Figure 1 "Test Data"), and the second signal to comprise of data strobe (Figure 1 "Strobe"), since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

As per claim 23:

Lin substantially teaches a memory module, comprising: a plurality of memory devices (Figure 2 # 50A-c); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 26); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device (Figure 4A); and a self-test module (Figure 1 # 22) coupled to at least one of the memory devices, the self-test module being operable to couple a series of corresponding first and second signals to the at least one memory device and to alter the relative timing between when some of the

corresponding first and second signals in the series are coupled to the at least one memory device over a range (Figure 1 # 24), the self-test module further receiving output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first and second signals (Figure 1 # 34), at least one input device coupled to the peripheral device port of the system controller (Figure 1 # 32); at least one output device coupled to the peripheral device port of the system controller (Figure 1 # 38) and at least one data storage device coupled to the peripheral device port of the system controller (Figure 1 # 30).

Lin does not explicitly mention that processor having a processor bus or a system controlled having a system memory port and a peripheral device port. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to realize that the apparatus taught in Lin generally includes standard equipment like a processor, processor bus, a controller, and various input/output ports. Therefore it would have been obvious to one with ordinary skill in the art at the time the invention was made to use the mentioned apparatus since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Further it should be noted that the tester (Figure 1 # 22) could be used within Lin's invention to perform the exact same functions as the apparatus mentioned in claim 23. Hence these should be considered as art recognized equivalents.

As per claims 32:

Lin substantially teaches a memory module, comprising: a plurality of synchronous memory devices (Figure 2 # 50A-C); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 26); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device (Figure 1 # 22); and a variable frequency clock generator producing and coupling to the at least one memory device a clock signal having a frequency corresponding to a frequency control signal (Figure 1 # 24); and a self-test module coupled to at least one of the memory devices, the self-test module being operable to generate the frequency control signal so that the frequency of the clock signal varies over a range (Figure 1 # 24, column 4, lines 15-65)), the self-test module further being operable couple a series of first input signals to the at least one memory device and to receive output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first signals as the frequency of the clock signal is varied (Figure 1 # 34), at least one input device coupled to the peripheral device port of the system controller (Figure 1 # 32); at least one output device coupled to the peripheral device port of the system controller (Figure 1 # 38) and at least one data storage device coupled to the peripheral device port of the system controller (Figure 1 # 30).

Lin does not explicitly mention that processor having a processor bus or a system controlled having a system memory port and a peripheral device port. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to realize that the apparatus taught in Lin generally includes standard equipment like a processor, processor bus, a controller, and various input/output ports. Therefore it would have been obvious to one with ordinary skill in the art at the time the invention was made to use the mentioned apparatus since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Further it should be noted that the tester (Figure 1 # 22) could be used within Lin's invention to perform the exact same functions as the apparatus mentioned in claim 23. Hence these should be considered as art recognized equivalents.

Claims 7-8, 24-31, 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable under Lin et al. US Pat no. 6880117 B2 and further in view of Sine et al. US Pat no. 5621739.

As per claims 7 & 8:

Lin substantially teaches a memory module, comprising: a plurality of memory devices (Figure 2 # 50A-c); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 26); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and

coupling read data from the memory device (Figure 4A); and a self-test module (Figure 1 # 22) coupled to at least one of the memory devices, the self-test module being operable to couple a series of corresponding first and second signals to the at least one memory device and to alter the relative timing between when some of the corresponding first and second signals in the series are coupled to the at least one memory device over a range (Figure 1 # 24), the self-test module further receiving output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first and second signals (Figure 1 # 34), wherein the self-test module comprises a memory sequencer coupled to the at least one memory device, the memory sequencer generating and coupling to at least one memory device a sequence of control signals to cause the at least one memory device to respond to each of the first and second signals in the series (Figure 2 # 48).

Lin does not explicitly teach the delay line coupled to the BIST.

However, Sine et al. in an analogous art teaches a delay line coupled to a BIST (Figure 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a delay line within the tester of Lin, since that would enable Lin's apparatus to make use of the benefits of delay testing. Further it should be noted that the timing generator/frequency multiplier (Figure 1) could be used within Lin's invention as a delay line. Hence these should be considered as art recognized equivalents.

As per claims 24-31:

These claims teach the same limitations as claims 2-10. Therefore these claims are rejected under the same basis as mentioned above.

As per claims 33-35:

These claims teach the same limitations as claims 20-22. Therefore these claims are rejected under the same basis as mentioned above.

As per claims 36-50:

Claims 36-50 are directed to a method of the system and memory modules of claims 1-35. Lin and Sine teach, either alone or in combination as stated above, the system and memory modules as set forth in claims 1-35. Therefore, Lin and Sine also teach, either alone or in combination as stated above, the methods as set forth in claims 36-50.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

Saqib Siddiqui
Art Unit 2138
01/07/2007

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